TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VHCT245AF,TC74VHCT245AFT,TC74VHCT245AFK

Octal Bus Transceiver

The TC74VHCT245A is an advanced high speed CMOS OCTAL BUS TRANSCEIVER fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It is intended for two-way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input ($\overline{G}$) can be used to disable the device so that the busses are effectively isolated.

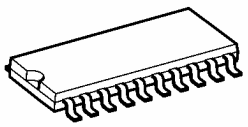
The input voltage are compatible with TTL output voltage.

This device may be used as a level converter for interfacing 3.3 V to 5 V system.

Input protection and output circuit ensure that 0 to 5.5 V can be applied to the input and output (Note) pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, hot board insertion, etc.

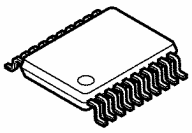
Note: Output in off-state

TC74VHCT245AF



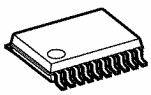
SOP20-P-300-1.27A

TC74VHCT245AFT



TSSOP20-P-0044-0.65A

TC74VHCT245AFK



VSSOP20-P-0030-0.50

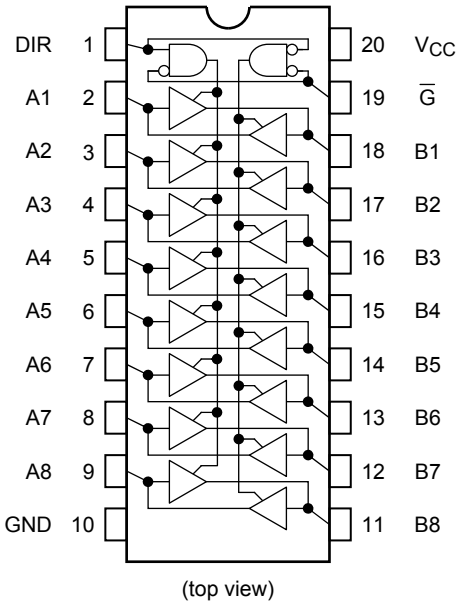
Weight
SOP20-P-300-1.27A : 0.22 g (typ.)
TSSOP20-P-0044-0.65A : 0.08 g (typ.)
VSSOP20-P-0030-0.50 : 0.03 g (typ.)

Features (Note)

- High speed: t_{pd} = 4.9 ns (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 4 μA (max) at Ta = 25°C
- Compatible with TTL outputs: V_{IL} = 0.8 V (max)
  V_{IH} = 2.0 V (min)
- Power down protection is provided on all inputs and outputs
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Low noise: V_{OLP} = 1.6 V (max)
- Pin and function compatible with the 74 series (74AC/HC/F/ALS/LS etc.) 245 type.

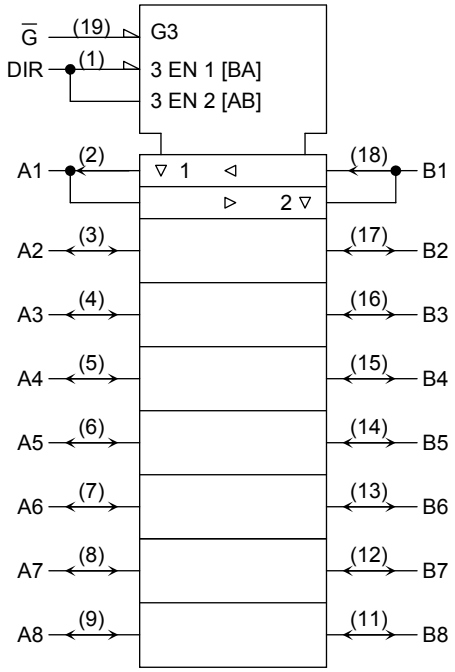
Note: Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

Pin Assignment



(top view)

IEC Logic Symbol



Truth Table

Inputs		Function		Output
$\overline{G}$	DIR	A Bus	B Bus	
L	L	Output	Input	A = B
L	H	Input	Output	B = A
H	X	Z		Z

X: Don’t care

Z: High impedance

Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating		Unit
Supply voltage range	V_{CC}	−0.5 to 7.0		V
DC input voltage (DIR, $\overline{G}$)	V_{IN}	−0.5 to 7.0		V
DC bus I/O voltage	$V_{I/O}$	−0.5 to 7.0	(Note 2)	V
		−0.5 to V_{CC} + 0.5	(Note 3)	
Input diode current	I_{IK}	−20		mA
Output diode current	I_{OK}	±20	(Note 4)	mA
DC output current	I_{OUT}	±25		mA
DC V_{CC}/ground current	I_{CC}	±75		mA
Power dissipation	P_D	180		mW
Storage temperature	T_{stg}	−65 to 150		°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: Output in off-state

Note 3: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 4: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Operating Ranges (Note 1)

Characteristics	Symbol	Rating		Unit
Supply voltage	V_{CC}	4.5 to 5.5		V
Input voltage (DIR, $\overline{G}$)	V_{IN}	0 to 5.5		V
Bus I/O voltage	$V_{I/O}$	0 to 5.5	(Note 2)	V
		0 to V_{CC}	(Note 3)	
Operating temperature	T_{opr}	−40 to 85		°C
Input rise and fall time	dt/dV	0 to 20		ns/V

Note 1: The operating ranges are required to ensure the normal operation of the device. Unused inputs and bus inputs must be tied to either VCC or GND. Please connect both bus inputs and the bus outputs with VCC or GND when the I/O of the bus terminal changes by the function. In this case, please note that the output is not short-circuited.

Note 2: Output in off-state

Note 3: High or low state

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
High-level input voltage	V_{IH}	—		4.5 to 5.5	2.0	—	—	2.0	—	V
Low-level input voltage	V_{IL}	—		4.5 to 5.5	—	—	0.8	—	0.8	V
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA	4.5	4.4	4.5	—	4.4	—	V
			I_{OH} = −8 mA	4.5	3.94	—	—	3.80	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	4.5	—	0.0	0.1	—	0.1	V
			I_{OL} = 8 mA	4.5	—	—	0.36	—	0.44	
3-state output off-state current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.25	—	±2.50	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	—	40.0	μA
	I_{CCT}	Per input: V_{IN} = 3.4 V Other input: V_{CC} or GND		5.5	—	—	1.35	—	1.50	mA
Output leakage current	I_{OPD}	V_{OUT} = 5.5 V		0	—	—	0.5	—	5.0	μA

AC Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	C_L (pF)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
Propagation delay time	t_{pLH} t_{pHL}	—	5.0 ± 0.5	15	—	4.9	7.7	1.0	8.5	ns
				50	—	5.4	8.7	1.0	9.5	
3-state output enable time	t_{pZL} t_{pZH}	R_L = 1 kΩ	5.0 ± 0.5	15	—	9.4	13.8	1.0	15.0	ns
				50	—	9.9	14.8	1.0	16.0	
3-state output disable time	t_{pLZ} t_{pHZ}	R_L = 1 kΩ	5.0 ± 0.5	50	—	10.1	15.4	1.0	16.5	ns
Output to output skew	t_{osLH} t_{osHL}	(Note 1)	5.0 ± 0.5	50	—	—	1.0	—	1.0	ns
Input capacitance	C_{IN}	DIR, $\overline{G}$			—	4	10	—	10	pF
Bus input capacitance	$C_{I/O}$	An, Bn			—	13	—	—	—	pF
Power dissipation capacitance	C_{PD}	(Note 2)			—	16	—	—	—	pF

Note 1: Parameter guaranteed by design.

$t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

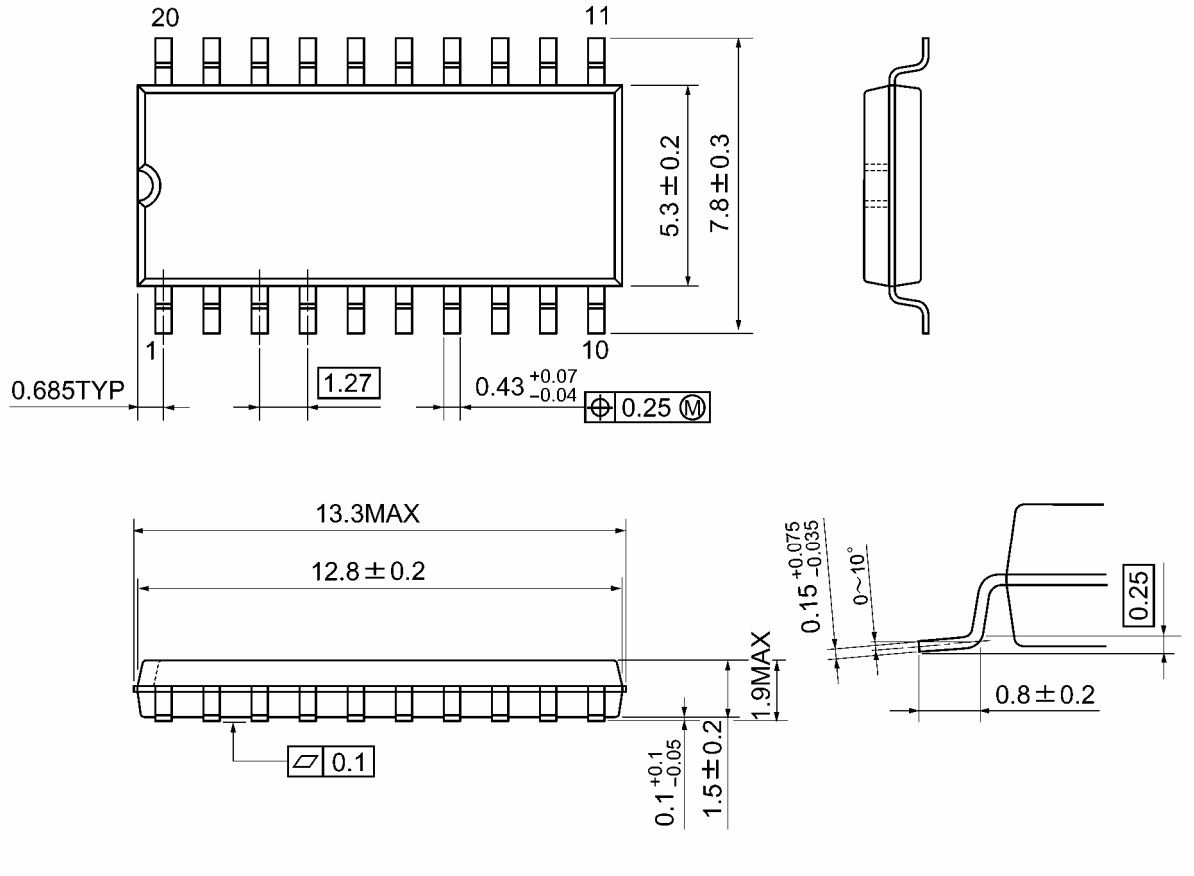
$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per bit)

Noise Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Unit
			V_{CC} (V)	Typ.	Limit	
Quiet output maximum dynamic V_{OL}	V_{OLP}	C_L = 50 pF	5.0	1.1	1.5	V
Quiet output minimum dynamic V_{OL}	V_{OLV}	C_L = 50 pF	5.0	−1.1	−1.5	V
Minimum high level dynamic input voltage	V_{IHD}	C_L = 50 pF	5.0	—	2.0	V
Maximum low level dynamic input voltage	V_{ILD}	C_L = 50 pF	5.0	—	0.8	V

Package Dimensions

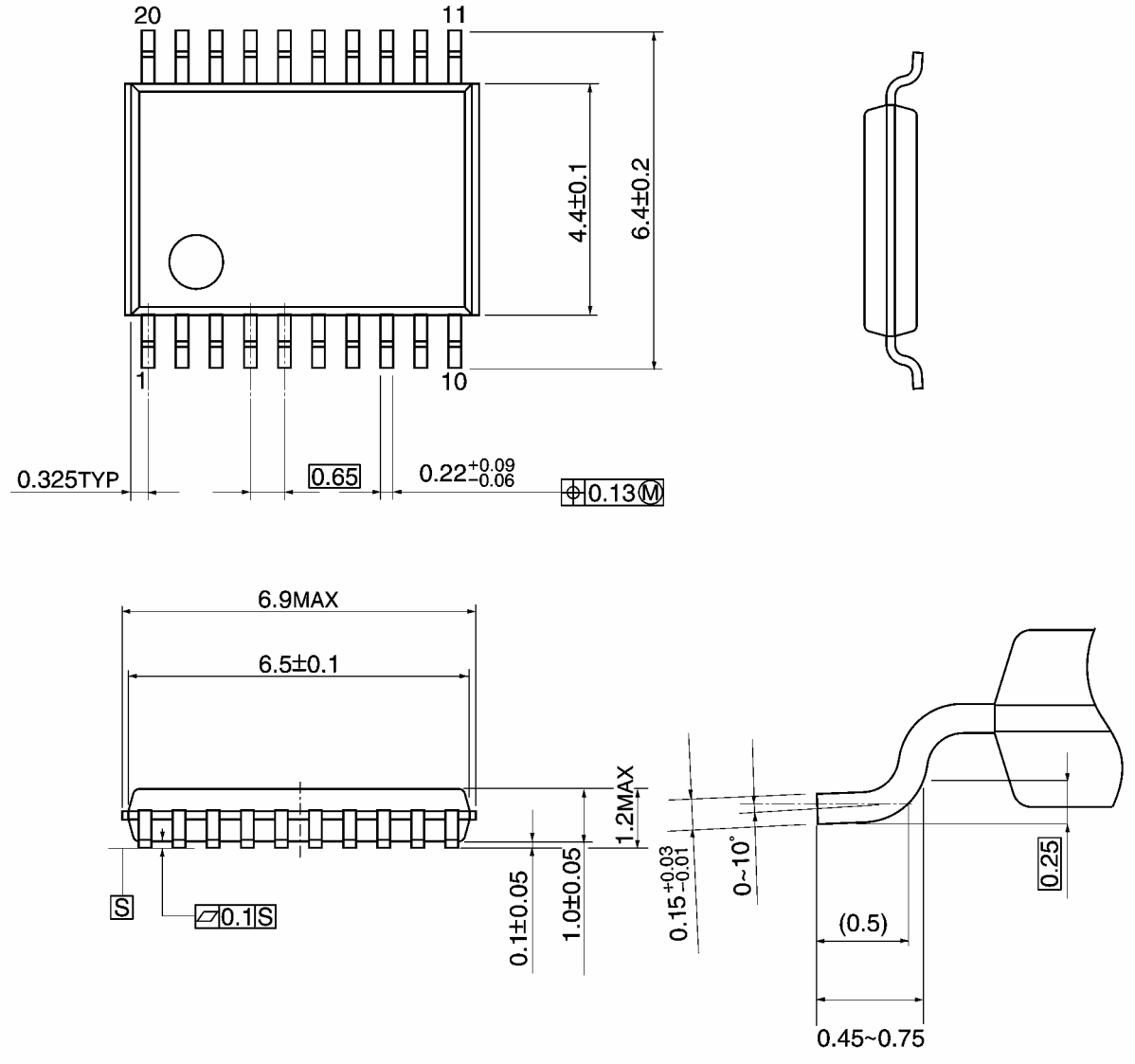
SOP20-P-300-1.27A Unit: mm



Weight: 0.22 g (typ.)

Package Dimensions

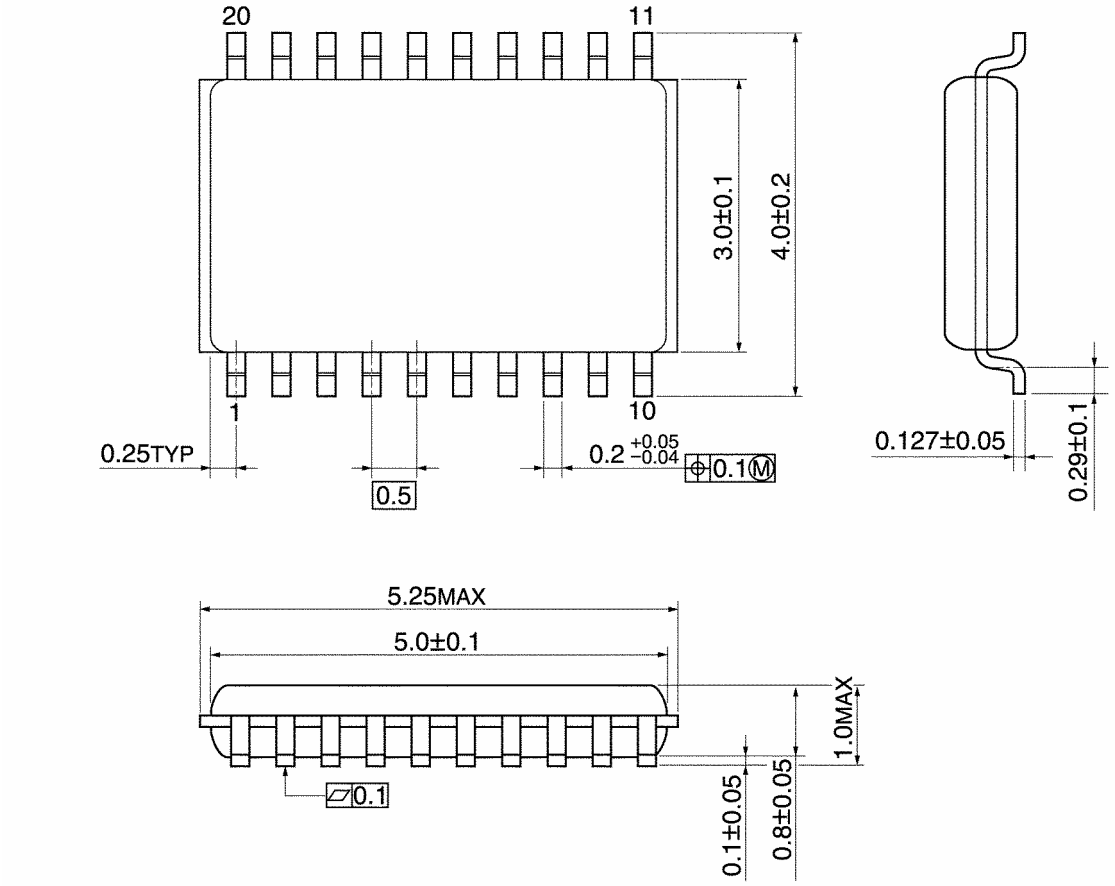
TSSOP20-P-0044-0.65A Unit: mm



Weight: 0.08 g (typ.)

Package Dimensions

VSSOP20-P-0030-0.50 Unit: mm



Weight: 0.03 g (typ.)

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